What is claimed is:

1. A phase-locked loop circuit comprising:

a DLL circuit having phase difference detecting means for detecting a phase difference between a reference clock signal and a synchronous clock signal to be supplied to an electronic circuit which operates in synchronization with said synchronous clock signal, and a phase difference changing means for, when a phase difference between the reference clock signal and the synchronous clock signal is detected by said phase difference detecting means, outputting a reference clock delay signal and a synchronous clock delay signal, with a predetermined phase difference being added, to increase the detected phase difference between the reference clock signal and the synchronous clock signal; and

a analog PLL circuit being supplied with said reference clock delay signal and said synchronous clock delay signal from said phase difference changing means, controlling the phase of an output control signal to synchronize said synchronous clock delay signal with said reference clock delay signal, and supplying the output control signal as said synchronous clock signal to said electronic circuit.

2. A phase-locked loop circuit according to claim 1, wherein said phase difference changing means sets the sum of said detected phase difference and said added predetermined phase difference to a value greater than a steady state phase error of said analog PLL circuit.

3. A phase-locked loop circuit according to claim 1, wherein said DLL circuit comprises:

a phase comparator for detecting the phase difference between said reference clock signal and said synchronous clock signal;

a first delay circuit for delaying said reference clock signal and outputting said reference clock delay signal;

a second delay circuit for delaying said synchronous clock signal and supplying said synchronous clock delay signal; and

a control circuit for being supplied with a signal representing the phase difference detected by said phase comparator, and controlling a delay time of at least one of said first delay circuit and said second delay circuit based on said signal representing the phase difference.

4. A phase-locked loop circuit according to claim 3, wherein said first delay circuit and said second delay circuit have respective maximum delay times set to a value which substantially corresponds to a steady state phase error of said analog PLL circuit.

5. A phase-locked loop circuit according to claim 3, wherein said control circuit is supplied with a plurality of detected results from said phase comparator, and if either one of the phases of said reference clock signal and said synchronous clock signal is more delayed than the phase of the other signal less than a predetermined number of times, then said control circuit increases the delay time of the delay circuit for delaying said other signal, and if either one of the phases of said reference clock signal and said synchronous clock signal is more delayed than the phase of the other signal said predetermined number of times or more, then said control circuit does not change the delay times of said first and second delay circuits, but keeps a present delay control action.

6. A phase-locked loop circuit according to claim 1, further comprising:

a CTS circuit having elements arranged and wired in a tree configuration for equalizing the phase of the output clock signal supplied from said analog PLL circuit and supplying the output clock signal as said synchronous clock signal to an input terminal of said electronic circuit.

7. A semiconductor integrated circuit incorporating therein said phase-locked loop circuit according to claim 1, said semiconductor integrated circuit being supplied with said reference clock signal from an external source.

8. A phase-locked loop circuit comprising:

an analog PLL circuit for comparing the phase of a first signal with the phase of a second signal and outputting a third signal; and

a DLL circuit being supplied with a reference signal and said third signal as a feedback signal, comparing the phase of said reference signal with the phase of said feedback signal, and outputting said first signal and said second signal based on a result of comparison between the phase of said reference signal and the phase of said feedback signal.

9. A phase-locked loop circuit according to claim 8, wherein said DLL circuit comprises;

a first delay circuit and a second delay circuit, each comprising a plurality of cascaded unit delay circuits, the arrangement being such that a first unit delay circuit of said first delay circuit receives said reference signal and a predetermined one of the unit delay circuits of said first delay circuit outputs

said first signal, and that a first unit delay circuit of said second delay circuit receives said feedback signal and a predetermined one of the unit delay circuits of said second delay circuit outputs said second signal.

10. A phase-locked loop circuit according to claim 9, wherein said first and second delay circuits have respective total delays each set to a value which substantially corresponds to the absolute value of a steady state phase error of said analog PLL circuit.

11. A phase-locked loop circuit according to claim 8, wherein said DLL circuit comprises;

a first delay circuit comprising a plurality of cascaded unit delay circuits, the arrangement being such that a first unit delay circuit of said first delay circuit receives said reference signal, a predetermined one of the unit delay circuits of said first delay circuit outputs said first signal and outputs said feedback signal as said second signal, and said first delay circuit has a total delay set to a value which substantially corresponds to the absolute value of a steady state phase error of said analog PLL circuit.